

FIG. 1

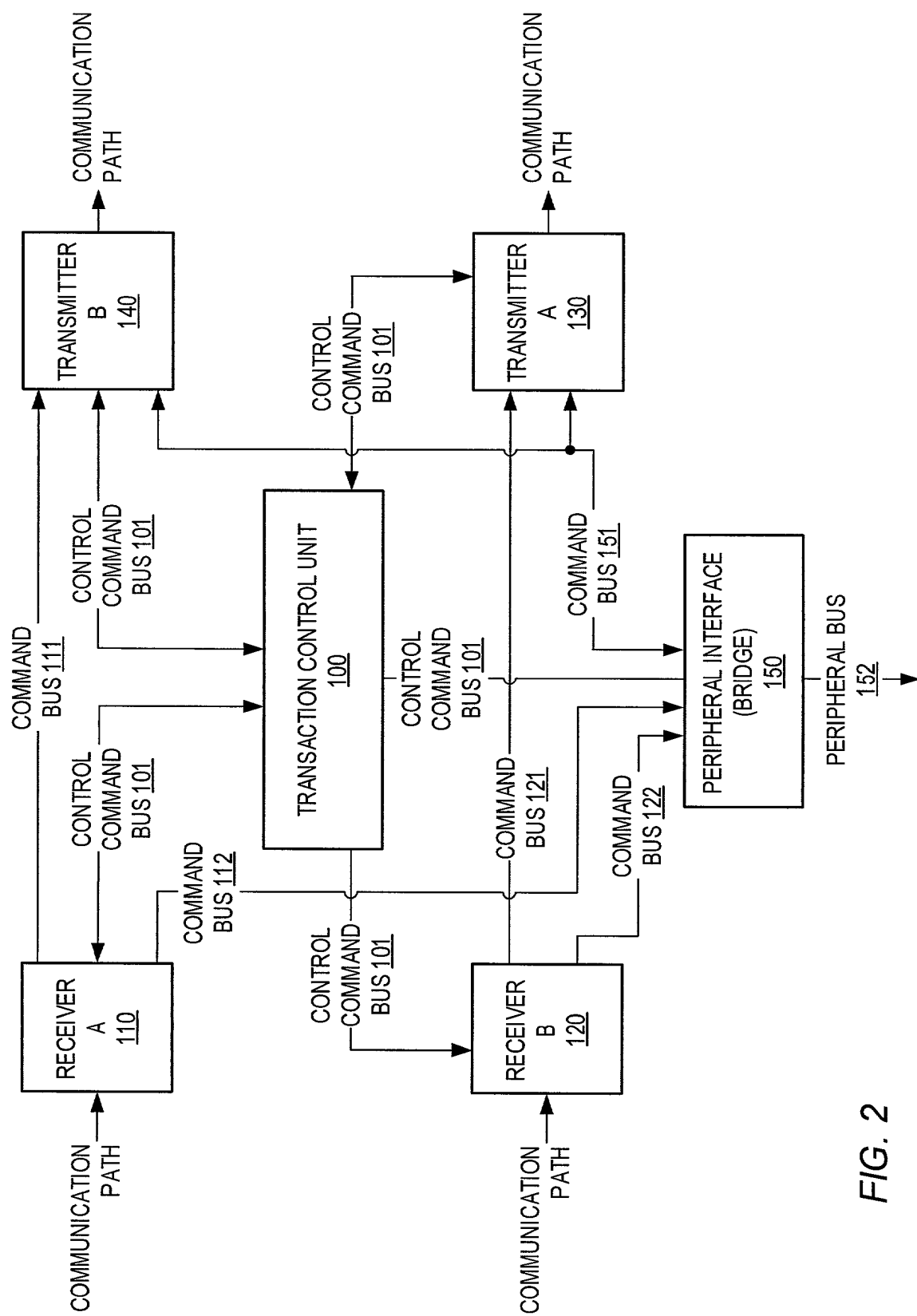


FIG. 2

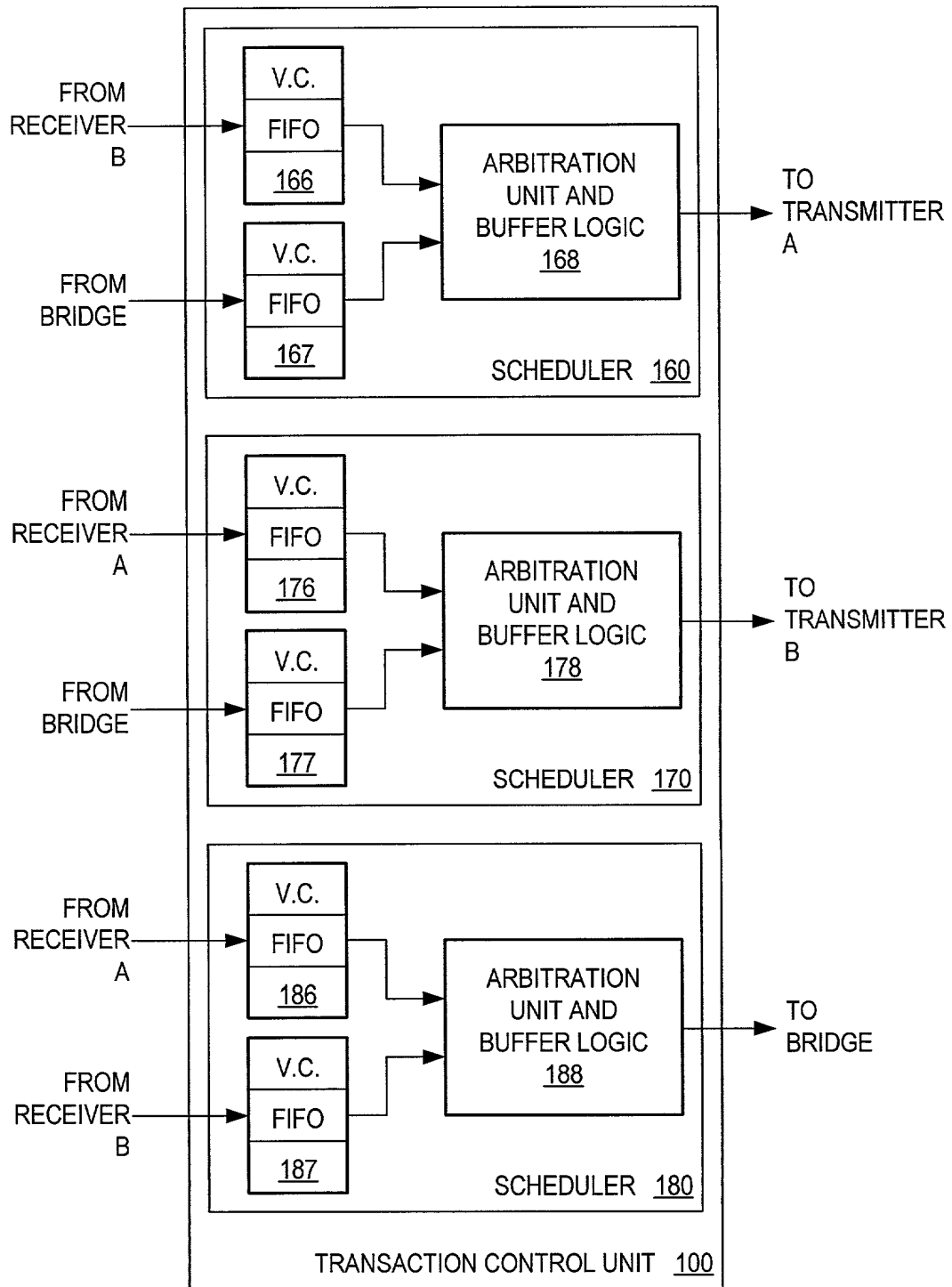


FIG. 3

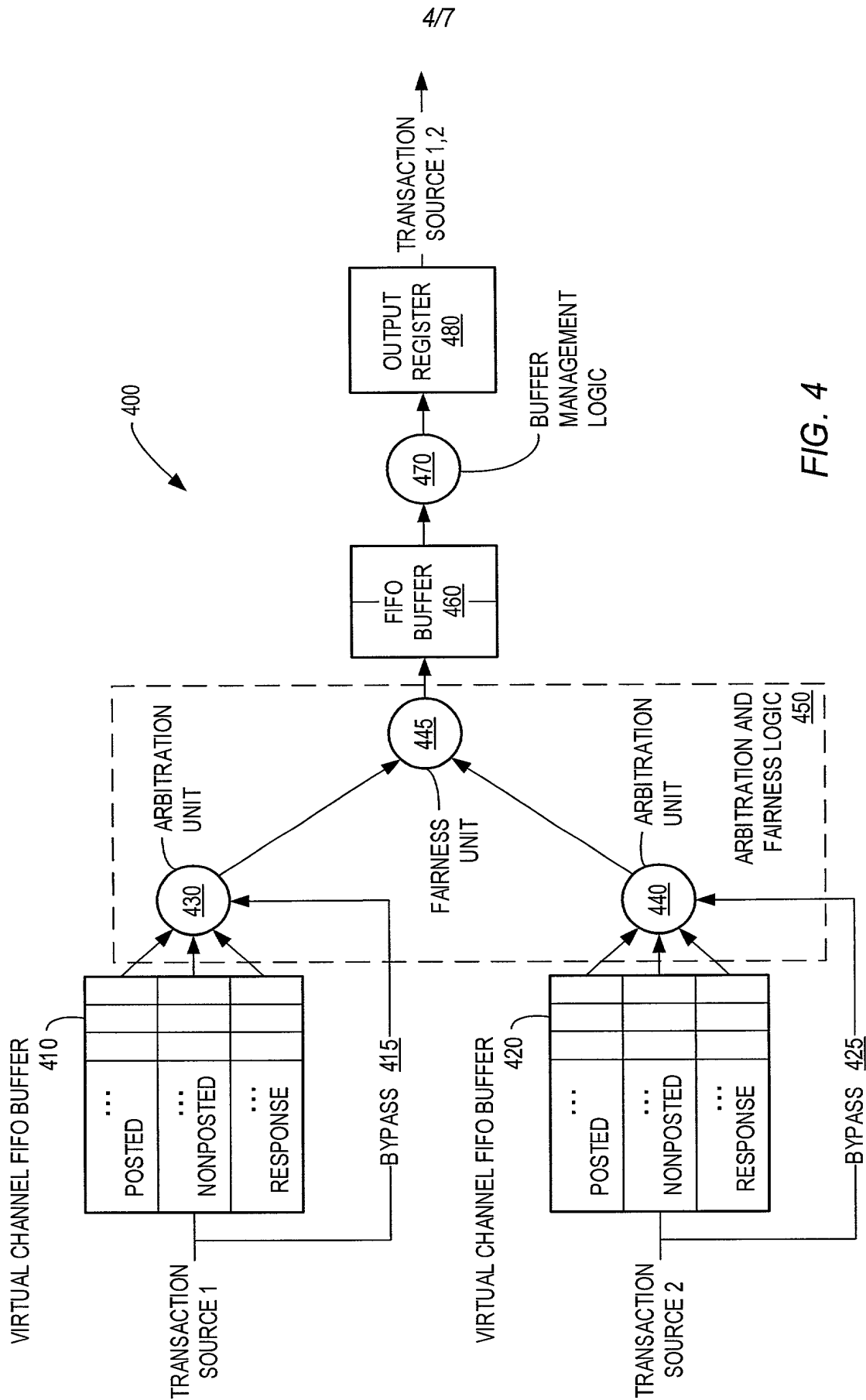


FIG. 4

FIG. 5 is a block diagram of a system for managing a virtual channel buffer. The system includes a control command input, a tagging logic unit (510), a virtual channel FIFO buffer (505), and a tag comparison/arbitration logic unit (520). The virtual channel FIFO buffer (505) is a table with columns R, NP, and P, and rows indexed 0 to 15. The tagging logic unit (510) receives a control command and outputs to the R and NP columns of the FIFO buffer. The tag comparison/arbitration logic unit (520) receives inputs from the R, NP, and P columns of the FIFO buffer and outputs a result. A detailed view of the FIFO buffer is provided in the table below.

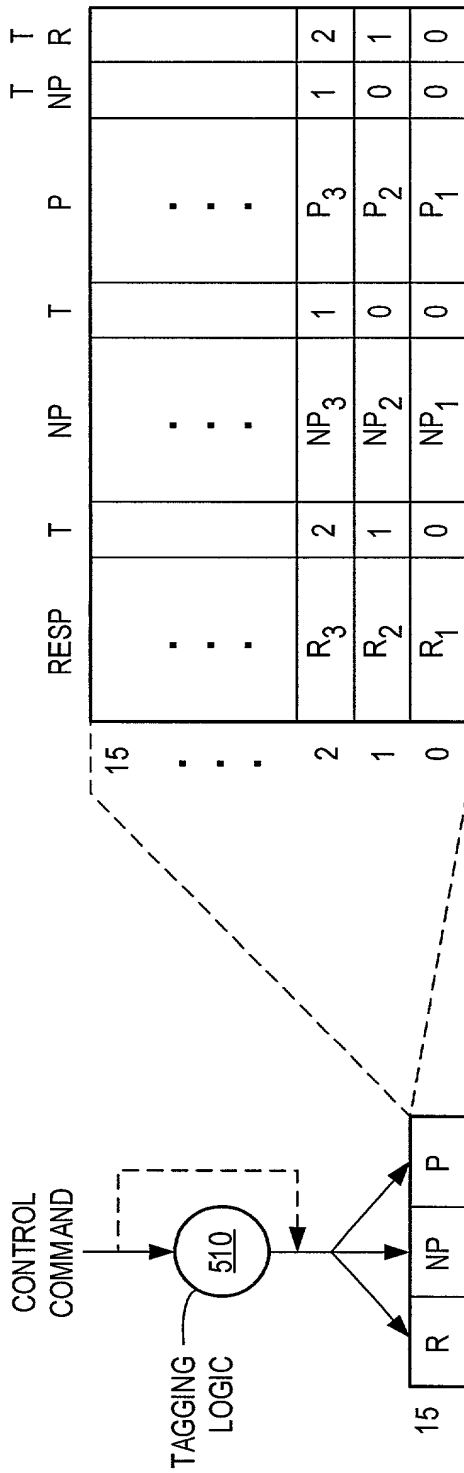


FIG. 5

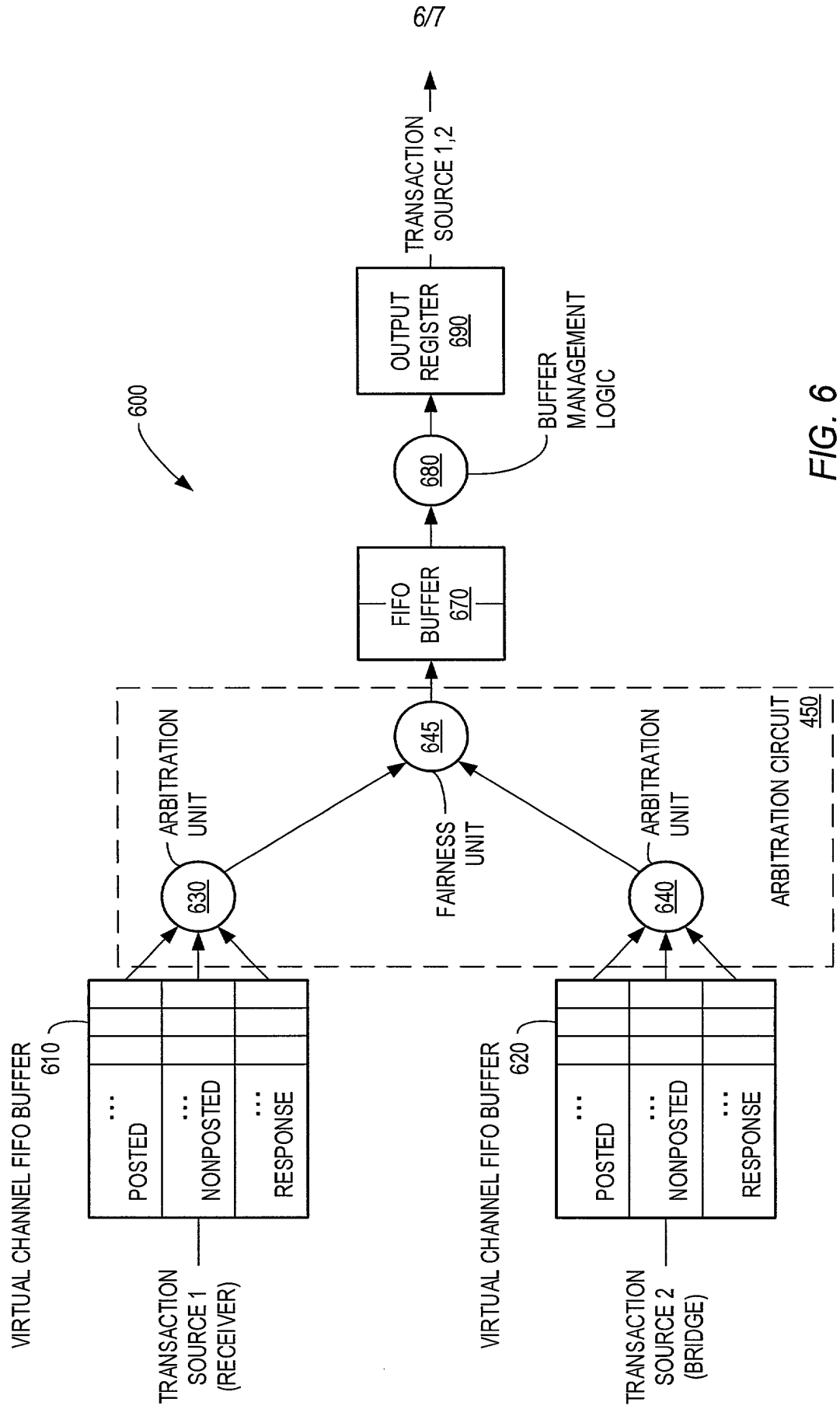


FIG. 6

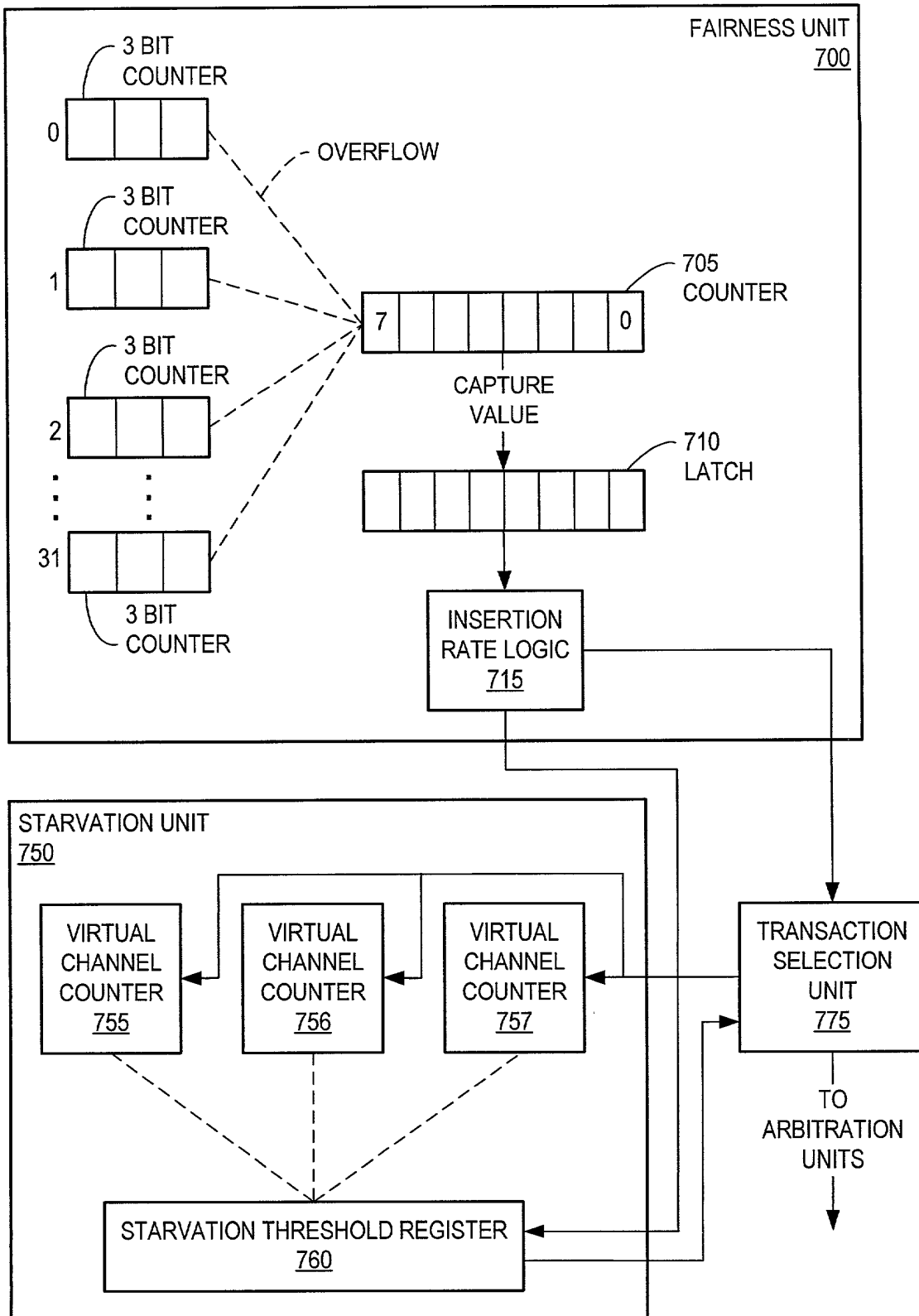


FIG. 7